IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) Method for producing a semiconductor device with the steps of:

   (a) applying an interconnect level to a semiconductor substrate;

   (b) structuring the interconnect level; [[and]]

   (c) applying a solder layer on the structured interconnect level in such a way that the solder layer assumes the structure of the interconnect level, so that the vertical extent of the solder layer corresponds to an interconnect structure of the interconnect level[[,]]; and

   (d) applying after the application of the structured solder layer, a non-conductive plastic, preferably polymer, in such a way that the tips of the solder balls for the vertical bonding protrude from the plastic, other solder structures being covered over.

2. (Previously Presented) Method according to claim 1, wherein the interconnect level is applied in a sputtering process or in a depositing process without external current.

3. (Previously Presented) Method according to claim 1, wherein the interconnect level which is applied comprises a metal, preferably copper and/or nickel and/or aluminum.

4. (Previously Presented) Method according to claim 1, wherein the interconnect level is structured with the aid of a photolithographic process.

5. (Previously Presented) Method according to claim 1, wherein a carrier layer which preferably comprises titanium and is structured like the interconnect level is applied on the semiconductor substrate.

6. (Previously Presented) Method according to claim 1, wherein the solder layer is applied in a printing process and is distributed in a predetermined way by re-liquefying or reflowing of the solder.

7. (Previously Presented) Method according to claim 1, wherein the solder layer is applied in a dip soldering process, in which the upper side of the semiconductor substrate provided with the structured interconnect level is dipped into a solder bath.

8. (Previously Presented) Method according to claim 1, wherein a solder resist layer is selectively applied on predetermined portions of the arrangement after the structuring of the interconnect level and before the application of the solder layer.

9. (Previously Presented) Method according to claim 1, wherein side walls of the structured interconnect level and/or of the carrier layer are wetted with solder.

10. (Previously Presented) Method according to claim 1, wherein both solder traces and solder balls for the bonding of further semiconductor devices and/or a printed circuit board in the vertical direction are formed during the application of the solder layer, preferably in the same process step.

11. (Canceled)

12. (Currently Amended) Method according to claim [[11]] 1, wherein the applied polymer is only cured during or after the electrical bonding with a further semiconductor device and/or a printed circuit board in the vertical direction.

13. (Currently Amended) Method according to claim [[11]] 1, wherein the polymer is applied in a printing process.

14. (Previously Presented) Method according to claim 1, wherein the conductive interconnect level is formed on the semiconductor substrate and/or contact

devices such as bonding pads in a printing or stamping process with a highly reactive substance, which comprises at least one noble metal, such as preferably platinum or palladium.

15. (Currently Amended) Semiconductor device with:

(a) a semiconductor substrate;

(b) a structured interconnect level on the semiconductor substrate; [[and]]

(c) a solder layer on the structured interconnect level for enlarging the conductive cross section, the solder layer assuming the structure of the interconnect level, so that the vertical extent of the solder layer corresponds to an interconnect structure of the interconnect level[[,]]; and

(d) wherein the structured solder layer has a solder layer height which corresponds approximately to half the structure width of the structured interconnect level.

16. (Previously Presented) Semiconductor device according to claim 15, wherein the structured interconnect level comprises a metal, in particular aluminum and/or copper.

17. (Previously Presented) Semiconductor device according to claim 15, wherein the structured interconnect level provides on the semiconductor substrate a carrier layer, which is structured like the interconnect level and preferably comprises titanium and/or copper.

18. (Previously Presented) Semiconductor device according to claim 15, wherein side walls of the structured interconnect level and/or of the carrier layer are wetted with solder.

19. (Previously Presented) Semiconductor device according to claim 15, wherein the semiconductor device is mechanically connected to at least one further semiconductor device and/or a printed circuit board by means of a

plastic or a polymer, the electrical connection being provided in the vertical direction by means of solder balls.

20. (Canceled)